

# VirtexII™-Based ASIC Prototyping Engine

## Features

- 32/64-bit, +3.3V, PCI/PCI-X based PWB
  - Available in configurations with two to five VirtexII™ FPGAs (FF1152 BGA)
  - Available with: 2V4000/2V6000/2V8000
  - Four 512Kx36 SSRAMS
  - One 72-Bit SDRAM DIMM (product ships with a 1 Gbyte SDRAM DIMM(PC133))
  - Tightly interconnected FPGA's facilitate the partitioning process.
- Flexible, abundant and configurable embedded memory in FPGA's:
  - Up to 1620 Kbytes dual-port Block SelectRAM (assuming 5 2V6000)
  - Up to 660 Kbytes Distributed SelectRAM (assuming 5 2V6000)

- 10A on-board switching regulator for both +3.3V and +1.5V (Only requires +5V power).
- Standalone operation via separate power connector.
- Status LED's provide instant status and operational feedback.
- 2 CY7B993/4 RoboClock II PLLs
- 2 3807 Clock Drivers
- Fast/Easy FPGA configuration via standard SmartMedia FLASH card:
  - Microprocessor controlled (ATmega 128L)
  - RS232 port for configuration and/or operational status and control
  - Fastest possible configuration using SelectMap
  - Five 2V6000s configure in under 5 seconds.

- Sanity checking programs for bit files simplify the configuration process.
- 5 low skew clocks distributed to all FPGAs and headers (from up to 8 possible sources)
  - 2 socketed oscillators
  - PCI clock
  - 1 clock dividable via CPLD
  - 4 external clocks via ribbon cable (may be differential!)
- Robust observation/debug with 400+ connections for logic analyzer observability and pattern generator stimulus.
- Custom daughter PWB headers for application-specific circuitry and interfaces.
- Full support for chipscope & Identify™

## Description

The DN3000k10 is a complete logic emulation system that enables ASIC or IP designers to prototype logic and memory designs for a fraction of the cost of other solutions. The DN3000k10 can either be hosted in a 32/64-bit PCI/PCI-X slot or used in a stand-alone environment. A single DN3000k10 configured with five 2V6000s can emulate up to 3 million gates of logic as measured by LSI (not including memories). The DN3000k10 achieves high gate density and allows for fast target clock frequencies by utilizing up to five FPGAs from Xilinx's VirtexII™ family for logic and memory. High I/O-count, 1152-pin, flip-chip BGA packages are employed, providing for abundant, fixed interconnect between FPGAs. Over 400 test pins are provided on top of the PWB for logic analyzer-based debugging and pattern generator stimulus. Custom daughter cards can be mounted to these connectors to interface the DN3000k10 to application-specific circuits. A reference 32-bit PCI target design and test bench are provided (in Verilog and VHDL) at no additional cost.



